R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 7 lines 7-19, page 8 lines 9-20, page 9 lines 1-13, page 11 lines 5-12 and FIGS. 2 and 3, as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 1-14 and 16-20 under 35 U.S.C. §112, second paragraph, for indefiniteness has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2, 14 and 16 under 35 U.S.C. §102(b) as being anticipated by Trauben et al. '130 (hereafter Trauben) has been obviated by appropriate amendment and should be withdrawn.

Trauben concerns a method and apparatus for grouping multiple instructions, issuing grouped instruction simultaneously, and executing groups instruction in a pipelined processor (Title).

Claim 1 provides (in part) a step for fetching a third instruction stored at a mispredict recovery address immediately

following a next address in response to determining not to take a branch. In contrast, FIG. 10b of Trauben appears to contemplate that a Sequential 1 instruction immediately following a DelayInst instruction (asserted similar to the claimed second instruction) is fetched prior to evaluating (e0) a branch condition, and thus not in response to determining not to take the branch as presently claimed. Therefore, Trauben does not disclose or suggest a step for fetching a third instruction stored at a mispredict recovery address immediately following a next address in response to determining not to take a branch as presently claimed. Claims 14 provides language similar to claim 1. As such, claims 1 and 14 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides (in part) a step for fetching a third instruction stored at a sequential instruction address immediately following a branch target address in response to determining to take a branch. In contrast, FIG. 10a of Trauben appears to contemplate that a Target 2 instruction immediately following a Target 1 instruction (asserted similar to the claimed second instruction) is fetched at the same time as the Target 1 instruction before a determination to take a branch is made. Therefore, Trauben does not disclose or suggest a step for fetching a third instruction stored at a sequential instruction address immediately following a branch target address in response to determining to take a branch as presently claimed. As such, claim

2 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 16 provides a step for storing a program counter address for a branch instruction in a stage of a pipelined processor for at least two pipeline cycles. In contrast, Trauben appears to be silent regarding storing a program counter address for a branch instruction in a stage of a pipelined processor for at least two pipeline cycles as presently claimed. Furthermore, the assertion on page 7, item 11 of the Office Action that the program counter address may have different values is inapplicable as the claim recites the program counter for the branch instruction, not any instruction. As such, claim 16 is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 3-6 under 35 U.S.C. §103(a) as being unpatentable over Trauben in view of Hennessy, pages 385 and 404 (hereafter Hennessy) is respectfully traversed and should be withdrawn.

The rejection of claims 7-11 under 35 U.S.C. §103(a) as being unpatentable over Trauben in view of Kahle '820 is respectfully traversed and should be withdrawn.

The rejection of claim 12, 13 and 17-20 under 35 U.S.C. §103(a) as being unpatentable over Trauben in view of Kahle and Hennessy is respectfully traversed and should be withdrawn

Trauben concerns a method and apparatus for grouping multiple instructions, issuing grouped instruction simultaneously, and executing groups instruction in a pipelined processor (Title). Hennessy concerns computer organization and design (Title). Kahle concerns processor and memory for separately predicting conditional branches dependent on lock acquisition (Title).

Clear and particular motivation to combine Trauben and Hennessy has not been established. In particular, the Office Action fails to provide particular findings as to the reasons a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited references for combination. The factual inquiry whether to combine references must be thorough and searching. The rigorous application of the requirement for showing the teaching or motivation to combine references is necessary to avoid the subtle but powerful attraction of a hindsight-based obviousness analysis. It is improper, in determining whether a person of ordinary skill in the art would have been led to the combination of references, simply to use that which the inventor taught against its teacher. Furthermore, the fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness (MPEP §2143.01). As such, because the Office Action fails to provide particular findings as to the reasons a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited references for combination, the Office Action does not appear to have met the Office's burden of factually establishing a *prima*

facie case of obviousness (MPEP §2142).

No clear and particular evidence of motivation to combine Trauben and Kahle has been established. In particular, the assertion on page 13, item d of the Office Action that minimizing stalls as taught bu Kahle would provide motivation appears to be a conclusory statement. Both FIGS. 10a and 10b of Trauben suggest that no stalls are experienced when branch prediction is correct or incorrect. Therefore, the asserted motivation to minimize stalls that do not exist does not appear to be correct. Therefore, *prima facie* obviousness has not been established for lack of clear and particular evidence of motivation to combine and/or modify the references. As such, the rejections of claims 3-13 and 17-20 should be withdrawn.

Claim 7 provides (in part) a circuit configured to present all of (i) a branch target address based on a branch instruction stored at a program counter address in prediction of taking a branch, (ii) a sequential instruction address having a first value immediately following the program counter address and (iii) a mispredict recovery address immediately following the sequential instruction address to a multiplexer in a single pipeline cycle. Despite the assertion starting on page 13, top paragraph of the Office Action, Kahle does not appear to discuss presenting all three of a branch target address, a sequential instruction address and a misprediction address to a multiplexer in a single pipeline cycle. In particular, column 5, lines 61-63 of Kahle state, "The address for the predicted path (e.g., **either** the

branch target address **or** the next sequential instruction address) forms an input of multiplexer 126." (Emphasis added). Kahle appears to contemplate providing only one address to a multiplexer. Furthermore, the text of Kahle cited by the Office Action does not appear to even mention providing a misprediction recover address to the multiplexer 126. Since a single address cannot anticipate three claimed addresses, the Office Action has failed to establish that Trauben and Kahle, alone or in combination, teach or suggest all of the claim limitations. As such, claim 7 is fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, Applicant's representative respectfully traverses the assertion on page 13 of the Office Action that a sequential address after a branch instruction address in inherently a recovery address for a branch misprediction. Inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981). As explained on page 9, lines 1-13 of the application, the MIPS ISA defines an address sequence having a conditional branch address, a branch delay slot address and a mispredict recovery address. Therefore, the MIPS ISA is an example where a sequential address (branch delay slot address) after a branch instruction address is not a misprediction recover address. As such, the inherency assertion should be withdrawn.

Regarding claim 12, the Office Action fails to provide evidence of a reasonable expectation of success. In particular,

the Office Action asserts on page 16, item C that Hennessy teaches "that **a sequential PC** is always computed **for every instruction**" (emphasis added). In contrast, page 23, item 41 of the Office Action admits Trauben teaches that multiple instructions have **"the same PC** for **each instruction** of the group" (emphasis added). A conflict appears to exist between Hennessy's approach of computing a sequential program counter address for every instruction and Trauben's approach of issuing multiple instructions having the same program counter. As such, the Examiner is respectfully requested to either (i) provide evidence of a reasonable expectation of success in view of the apparent conflict or (ii) withdraw the rejection for claim 12.

Claim 13 provides a structure including an exception program counter for storing an exception program counter address used in generating a mispredict recovery address having a second value proximate a program counter address. In contrast, each of Trauben, Kahle and Hennessy (pages 385 and 404) appear to be silent regarding an exception program counter for storing an exception program counter address used in generating a mispredict recovery address having a second value proximate a program counter address as presently claimed. Furthermore, the Office Action cites page 506 of Hennessy for teaching an exception program counter. However, page 506 of Hennessy is not on record as part of the ground of rejection. See PTO-892 form enclosed with the Office Action. Therefore, the Examiner is respectfully requested to

either (i) modify the grounds of rejection to include page 506 of Hennessy and provide a copy to Applicant or (ii) withdraw the rejection for claims 13, 19 and 20.

Claim 17 provides an incrementor coupled to a prefetch program counter. In contrast, none of Trauben, Hennessy or Kahle appear to mention an incrementor. Therefore, Trauben, Hennessy and Kahle, alone or in combination, do not teach or suggest an incrementor coupled to a prefetch program counter as presently claimed.

Furthermore, Applicant's representative respectfully traversed the assertion on page 19, item 27 of the Office Action that an incrementor in inherent. Inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981). Column 2, lines 43-45 of Trauben state that some instructions are variable in length. A non-incrementing approach is necessary for variable length instruction sets to update a corresponding program counter. Since the non-incrementing approach may be used for the fixed length instructions desired by Trauben, an incrementor is not certain in Trauben and thus not inherent. Claim 19 also provides an incrementor. As such, claims 17 and 19 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 18 provides a structure that includes an adder (i) coupled to both a prefetch program counter and an instruction

register and (ii) configured to generate a branch target address by adding an program counter address to an address displacement of a branch instruction. In contrast, none of Trauben, Kahle and Hennessy appear to teach or suggest an adder as presently claimed. Therefore, *prima facie* obviousness has not been established and the rejection should be withdrawn.

Furthermore, Applicant's representative respectfully traverses the assertion on page 20, top paragraph of the Office Action that adding a program counter address to an offset to generate a branch target address is inherent. MPEP §2112 states:

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. " *Ex parte Levy* 17 USPQ2d 1461, 1464, 1464 (Bd. Pat. App. & Inter. 1990)(emphasis in original)

However, the only "evidence" provided in the Office Action that adding necessarily flows from the teachings is a statement that "an absolute address is not taken". The statement is not supported by any evidence or technical reasoning from the references. Therefore, the statement appears to be conclusory and inherency has not been established. As such, the Examiner is respectfully requested to either (i) provide a basis in fact and/or technical reasoning to reasonably support a determination that all branch target addresses must be computed per the teachings of the applied prior art or (ii) withdraw the rejection.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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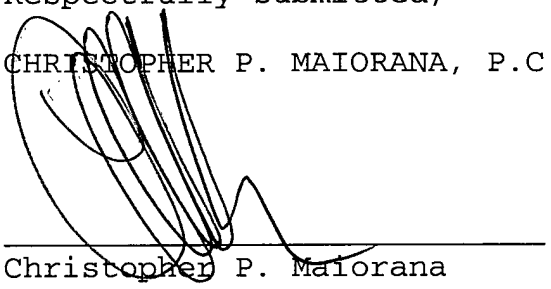

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Dated: November 15, 2004

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Docket No.: 00-419 / 1496.00055